Polycrystalline Si thin-film solar cells with absorber layers grown at temperatures below 600°C by ECRCVD

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Abstract: Solar cells were prepared with absorber layers grown below 600 °C on both polycrystalline Si seed layers on glass and Si(100) wafers. The seed layers were formed by the aluminum-induced layer exchange process (ALILE) based on the aluminum-induced crystallization of amorphous Si. To form a p-type absorber layer (~2 µm) the seed layers were thickened by ECRCVD using silane and diborane. A thin, highly phosphorous-doped amorphous emitter layer was deposited. We discuss the influence of absorber layer post-treatments on the solar cell parameters. We achieved open-circuit voltages of up to 378 mV for solar cells on seed layers by the application of defect annealing and hydrogen passivation. On highly-doped, p-type CZ-Si(100) we obtained an open-circuit voltage of 458 mV even without any additional treatments of the absorber layer. These results are very encouraging for low-temperature preparation of solar cells.
Key Words: Silicon, Thin-film Solar Cells, Seed Layer, Low-temperature Epitaxy, ECRCVD.

1 Introduction

An attractive low-temperature route to a polycrystalline Si (poly-Si) thin-film solar cell on a low-cost substrate like glass bases on the seed layer concept. In such a cell concept, we use a thin large-grained poly-Si seed layer on glass formed by aluminium-induced crystallisation (AIC). The absorber layer is grown on this seed layer in a subsequent epitaxial deposition process. The substrate temperature during growth is limited by the glass to temperatures below 600 °C. Electron-cyclotron resonance chemical vapour deposition (ECRCVD) can be used at such low temperatures to provide additional non-thermal energy to the surface of a growing film and realise therefore epitaxial growth of Si [1,2]. The additional use of a low-temperature emitter concept like an amorphous Si (a-Si:H) emitter allows to prepare solar cells on glass with a complete low-temperature process. In this paper, we present results of such solar cells and their performance is compared with reference cells grown on p^+-type Si(100) wafers.

2 Specimen Preparation

We prepared solar cells on both poly-Si seed layers on glass and p^+-type CZ-Si (100) wafers (2-5 mΩcm). The seed layers were prepared by the aluminium-induced layer exchange (ALILE). Details of this preparation can be found in [3]. The resulting poly-Si film (about 200 nm) on glass is p^+-type due to doping with Al. It is characterised by large grains (about 20 µm) and a (100) preferential orientation [about 75% of all grains are tilted less then 20° relative to (100)] [4].

The crystalline Si absorber layers were grown in an ECRCVD system with a RR 250 PQ (Roth & Rau, Germany) plasma source decomposing silane (SiH_4) and diborane (B_2H_6) by an H_2 plasma. The substrate temperature was about 590 °C. The resulting growth rate amounted to 20 nm/min. More details can be found elsewhere [2].

The substrate/p^-/n^+ solar cell test structures were prepared using a slightly boron-doped ECRCVD grown absorber on either the seed layer or the Si wafer. A highly phosphorous doped hydrogenated a-Si layer was deposited as standard emitter (thickness: 20 nm). A ZnO:Al film, about 80 nm thick, was used as a transparent conducting oxide layer. Device separation (mesa-etching) and metal grid definition (Al lift-off) was realised by photolithography. The cells had a non-interdigitating grid and a cell area of about 4×4 mm².

3 Results

Structural investigations of the absorber layers revealed a high defect density in the range of 4 x 10^8 cm² (extended defects on layer surface) [5]. It is a well known fact, that the presence of crystal defects influencing the performance of an electrical device can be reduced by post-deposition treatments of the Si films. For instance high-temperature annealing can improve the structural quality of such a film by rearranging the crystal structure. The limitation to temperatures below 600°C for all process steps by the glass substrate generally does not allows such treatments. Only very short annealing treatments as in rapid thermal annealing (RTA) processes can be applied. A second possibility of the reduction of electrically active defects in the Si films is the passivation of such defects by hydrogen. We applied both treatments to the Si films grown on seed layers, a short high-temperature annealing (850°C, 4 min) and plasma-hydrogen passivation (400°C, 15 min) in a plasma- enhanced chemical vapour deposition (PECVD). As can be seen in Fig.1, these treatments lead to a strong improvement of the solar cell performance.

In the Fig.1, the influence of post-deposition treatments of the absorber on the open-circuit voltage (V_{OC}) for two levels of absorber doping (SiH4 to B2H6 ratio) is shown. On ALILE seed layers (circles), as-grown V_{OC} of 61 mV and 284 mV were obtained with 5 ppm and 200 ppm, respectively. A defect annealing step prior to the emitter deposition resulted in the case of low doping in an increase of V_{OC} from 61 mV to 106 mV. The V_{OC} was further increased to 233 mV by an additional hydrogen passivation step. This shows clearly that additional treatments (defect annealing and defect passivation) are necessary to obtain reasonable open circuit voltages. Under such aspect, the as-grown V_{OC} of 284 mV obtained at the higher doping level is a very promising result. For comparison, using IAD for the epitaxial growth of the absorber an as-grown V_{OC} of 220 mV was reported recently [6]. As can be seen also in Fig.1, the additional treatments and the optimisation of the doping level led to a further increase of V_{OC}. For a solar cell with 100 ppm absorber doping a V_{OC} of 296 mV was obtained after the hydrogen passivation. An additional annealing step increased this value to 378 mV. These results are very promising, because the used treatment procedures were not optimised so far.

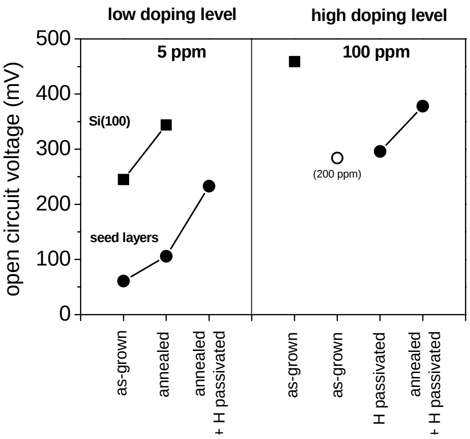

Fig.1 Open circuit voltage V_{OC} of thin-film solar cells with different absorber doping levels grown on ALILEn seed layers (circles) and Si (100) wafers (squares) with a boron doping ($[B_2H_6]/[SiH_4]$) of 5 ppm and 100 ppm (open circle: 200 ppm). The substrate/absorber stacks have been treated differently as indicated in the figure (annealing: 850°C, 4 min; H-passivation 400°C, 15 min)

Fig.1 also includes the results obtained for the reference system on Si (100) (squares). As can be seen, the as-grown V_{OC} of the solar cells with the low doping level increases from 245 mV to 344 mV by a defect annealing treatment. At a higher doping level (100 ppm) we obtained a V_{OC} of 458 mV even without any treatment of the absorber layer.

The corresponding I-V curves of the solar cells are presented in Figs. 2 and 3. In Fig.2, the I-V curve of the best solar cell on a seed layer is shown, where both treatments were applied. The cell results are V_{OC}=378 mV, J_{SC}=6.2 mA/cm², FF=43%, η=1.0%. Due to the non-interdigitated mesa-etched cell design the cells are still characterised by a strong series resistance.

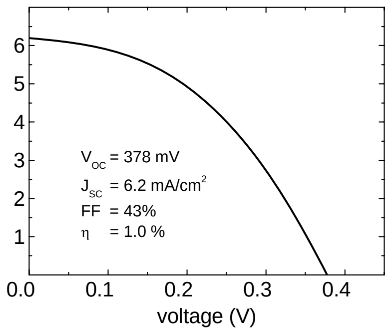

Fig.2 Current-voltage characteristic of a solar cell consisting of an about 2 µm thick epitaxially grown absorber layer on a poly-Si seed layer on glass. The absorber was treated by defect annealing and hydrogen-passivation

For comparison, in Fig.3 the I-V curve of a solar cell on Si (100) is shown. The efficiency of this cell is 4.2% at a V_{OC} of 458 mV, a J_{SC} of 13.0 mA/cm² and a FF of 71%. The results, especially J_{SC}, are very encouraging under the aspect of the only 2 µm thin absorber layer and absence of any light-trapping. In comparison to the cells on the seed layers the series resistance is strongly decreased due to the p^+ Si wafer. This shows, that an optimisation of the cell design can easily improve the cell performance (FF) on the seed layers.

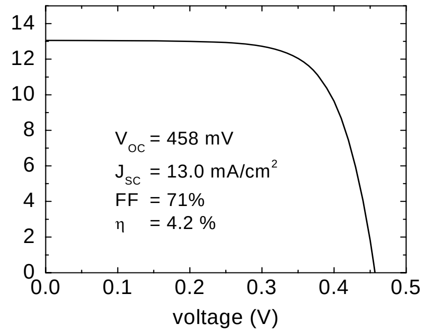

Fig.3 Current-voltage characteristic of a solar cell consisting of an about 2 µm thick epitaxially grown absorber layer on a p^+ type Si (100) wafer (reference system)

4 Summary and Conclusions

By following a seed layer concept, crystalline Si thin-film solar cells were prepared in a complete low-temperature process on both glass and Si-wafers. For that, we used a poly-Si seed layer on glass or a Si (100) wafer as templates for the epitaxial growth of the absorber layer by ECRCVD. An a-Si:H emitter layer was used to form the pn-junction. Encouraging open-circuit voltages of up to 378 mV were achieved on the seed layers by the application of defect annealing and hydrogen passivation, especially under the aspect that these treatments as well as the absorber doping level have not been optimised so far.

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