ADVANCED CONCEPTS FOR THIN-FILM POLYCRYSTALLINE-SILICON SOLAR CELLS

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ABSTRACT: Thin-film polycrystalline-silicon (pc-Si) solar cells could lower the price of photovoltaic energy if sufficiently high efficiencies are obtained. In the framework of the European FP6 project ATHLET, we are developing a pc-Si solar cell technology in which absorber layers are made by the creation of a pc-Si seed layer on a foreign substrate followed by epitaxial thickening. So far, we have reached cell efficiencies of up to 8.0% and V_{oc} values of up to 540 mV by using aluminium-induced crystallization in combination with high-temperature chemical vapor deposition on ceramic alumina substrates. In this paper we address some of the challenges that await us to further improve our pc-Si cell efficiency. We tested nanotextured Borofloat and glass-ceramic substrates and found them compatible with our intermediate- and high-temperature approaches respectively. We showed that high-quality AIC layers can be made on TCO-covered glass, which is an important result in view of obtaining cells in superstrate configuration. We grew absorber layers by different epitaxial deposition methods and found out that our cell efficiency is mainly limited by the presence of intragrain defects. We obtained cells in superstrate configuration V_{oc} values of up to 484 mV. The high current density obtained with our first pc-Si mini-module shows that our approach leads to homogeneous pc-Si layers.
Keywords: Polycrystalline-Silicon, Thin-Film, Crystallization

1 INTRODUCTION

The PV-market is dominated by wafer-based crystalline Si solar cells with a number of thin-film technologies challenging this dominant position. One of the emerging thin-film approaches in Europe as described in the European strategic research agenda for emerging and novel PV-technologies is the polycrystalline-silicon (pc-Si) thin-film approach. The grain size of these polycrystalline silicon layers is typically in the range of 0.1 to 100 μm and they can be deposited on inexpensive foreign substrates like glass or ceramics.

In the framework of the European FP6 project ATHLET, we are developing a pc-Si solar cell technology in which the pc-Si layers are made by a seed layer approach [1]. First, thin but large-grained seed layers are made by aluminium-induced crystallization (AIC) [2] or laser crystallization of amorphous silicon. These seed layers are then epitaxially thickened into absorber layers. Two different temperature regimes for epitaxial growth are under investigation: an intermediate-temperature regime up to 600˚C (e.g. e-beam evaporation and layered laser crystallization) and a high-temperature regime with deposition temperatures up to 1100˚C (e.g. thermal chemical vapor deposition). We have so far reached an efficiency of 8.0% for cells in substrate configuration made by AIC in combination with thermal CVD on ceramic alumina substrates [3-4]. This is by far the highest efficiency for pc-Si cells based on a seed layer approach but is not yet high enough to lead to a cost-effective PV technology.

In this paper we address some of the challenges that await us to further improve the efficiency of pc-Si solar cells made by a seed layer in combination with epitaxy. We will focus on work related to substrate development, seed and absorber layer deposition, and cell and module technology.

2 EXPERIMENTAL

We made pc-Si films on various substrates by epitaxial thickening of AIC seed layers. For the intermediate temperature approach, we used bare or ZnO-coated Borofloat® glass as substrates. For the high-temperature route, alumina substrates (CoorsTek ADS996) and glass-ceramic substrates (Corning Code 9664) were used. The alumina substrates were covered by a spin-on flowable oxide (FOx-25 from Dow Corning) to reduce their surface roughness, prior to the seed layer formation [5]. Al and a-Si layers were deposited by DC magnetron sputtering or by e-beam evaporation for the intermediate and the high-temperature route respectively. The substrate/Al/a-Si stacks were then annealed in tube furnaces at an annealing temperature between 425°C and 525˚C in N_2 ambient to obtain crystallization and layer exchange. Absorber layers were deposited on the AIC layers by electron-beam evaporation (intermediate-temperature route) or by thermal CVD (high-temperature route) or by layered laser crystallization (LLC).

3 RESULTS AND DISCUSSION

This section first describes two different kinds of glass substrates that we will use in the future to obtain pc-Si solar cells in superstrate configuration. Secondly, it shows that high-quality AIC seed layers can be obtained on glass substrates coated with a transparent conductive oxide (TCO), which is an important result in view of obtaining cells in superstrate configuration. Thirdly, this section discusses three different ways for epitaxial thickening of the seed layers. At present, intragrain defects in the absorber layers seem to be the main limiting factor of our pc-Si solar cell efficiency. Finally, it presents our first results on pc-Si cells in superstrate configuration and on pc-Si mini-modules.

3.1 Substrate development

To be able to make pc-Si solar cells in superstrate configuration, we have started to investigate the compatibility of different types of glass with our pc-Si processes and ways of texturing these glass substrates for light confinement purposes. Glass is a low cost substrate widely used for silicon thin film technologies. Due to its good transparency in the visible-NIR region, glass substrates enable to make silicon solar cells in both substrate and superstrate configuration. For our pc-Si thin-film approach, the most commonly used glass substrates like soda lime glass and borosilicate glass are at best only compatible with the intermediate-temperature regime due to their relatively low thermal stability. For the high-temperature regime, glass-ceramic substrates with a strain point above 900°C were investigated.

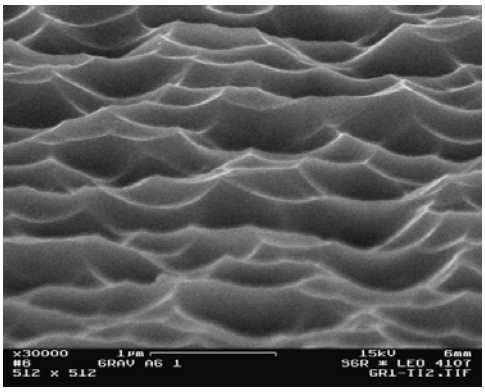

Figure 1: SEM image of the roughest (σ_{RMS}=81 nm) nanotextured borosilicate glass tested as substrate for AIC seed layers.

In the intermediate-temperature regime, we already succeeded in preparing pc-Si solar cells in substrate configuration on Borofloat® 33 glass from Schott, indicating that these substrates are thermally compatible to our intermediate-temperature process. To make pc-Si cells in superstrate configuration, a light-trapping nanotexture should be created on the surface of these glass substrates. This we recently achieved using a fluorinated plasma etching process where silver nodules are used as mask [6-7]. Since the AIC process is influenced by the substrate surface roughness [8], nanotextured borosilicate glass substrates with different texture roughness were prepared to evaluate whether the AIC process was compatible with these different surface textures. Textures with RMS roughnesses going from 10 nm to 81 nm have thus far been tested. Fig. 1 shows a typical SEM image of the tested nanotextures that show wavy surfaces with a pattern projection size around 500 nm. Various depths of the texture have been obtained controlling the plasma etching time.

AIC seed layers grown on these nanotextured glass substrates using standard conditions were all continuous and showed grain sizes larger than 5 µm. The glass texture is still present under the seed layer. Before epitaxial deposition, the seed layers of the intermediate-temperature route are polished by chemical-mechanical polishing (CMP). For the very rough samples however, it is difficult to end up with a smooth pc-Si surface without holes after CMP. First solar cells in superstrate configuration will therefore be processed in the near future on glass substrates with a rather smooth texture.

For the high-temperature route, the glass substrates we investigated are Code 9664 glass-ceramics from Corning Inc [9]. These substrates are first produced as glass sheets and then thermally treated to form a ceramic phase. The result is a transparent substrate with a strain point above 900˚C, that can withstand processing at 1130ºC during a sufficiently long period of time for the epitaxial deposition in our high-temperature route. The thermal expansion coefficient of these glass-ceramic substrates is closely matched to that of silicon.

We made pc-Si solar cells in substrate configuration on these glass-ceramics that showed a maximum efficiency of 6.4% [10]. While the V_{oc} and the fill factor of our best cells are comparable to those on alumina substrates, the J_{sc} is much lower for cells on glass-ceramic than for cells on alumina. This is the result of the much better diffuse back reflectance of the alumina substrates compared to the glass substrates. Our cell efficiency of 6.4% is the highest efficiency for pc-Si solar cells on glass based on the AIC process. These results indicate that the glass-ceramic substrates are fully compatible with our high-temperature pc-Si solar cell process.

3.2 Seed layer formation

An appealing option for the intermediate-temperature route is to form the seed layer on a TCO-coated glass substrate. This would allow for simplified contacting of the thin film solar cells in superstrate configuration.

We recently managed to form continuous AIC seed layers on ZnO:Al coated glass [11]. Raman measurements showed that these layers had a high-quality crystalline structure. Figure 2 compares the Electron Back Scatter Diffraction (EBSD) maps of AIC layers formed at 425˚C on ZnO:Al coated glass (a) and on bare glass (b). The maximum and the average grain sizes of the pc-Si films on ZnO:Al are 16 µm and 5 µm respectively. The grain size on ZnO:Al is therefore slightly smaller than that on bare glass (maximum size of 18 µm and average size of 7 µm). Higher annealing temperatures lead to smaller grain sizes for both substrate types. On both substrates, a preferential (001) orientation was observed (see the red color in Fig. 2). The fraction of the pc-Si surface showing an orientation within 20˚ of the (001) direction is about 60% for both substrate types. This preferential (001) orientation is very advantageous for epitaxial thickening of the absorber layer in the intermediate-temperature route (see section 3.3) [12].

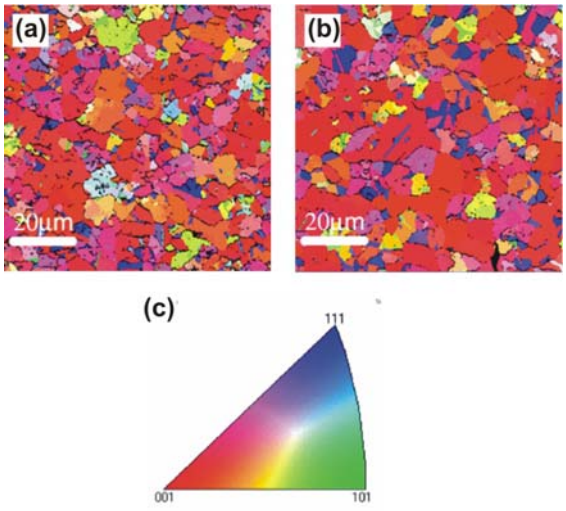

Figure 2: EBSD orientation maps of AIC layers on ZnO:Al coated glass (a) and on bare glass (b). The color scale for the orientation maps is shown in (c). The AIC layers were both annealed at 425˚C for 16 hours after which they received a CMP treatment to remove the top Al layer [11].

3.3 Absorber layer growth and characterization

We recently showed that the V_{oc} values of pc-Si solar cells made by the high-temperature route on alumina are almost independent of the grain size [13, 14]. By performing defect etching on our pc-Si layers, we found a very high intragrain defect density of around 10^9 cm^{-2} in our layers [15]. Figure 3 shows a top view SEM image of a defect-etched pc-Si layer. This layer had larger grains than our standard pc-Si layers used to achieve the 8.0% cell efficiency, but did not lead to higher V_{oc} values [13]. We used this large-grained pc-Si layer because intragrain defects are more easily detectable when dealing with large grains. We note however that similar results are obtained after defect etching of our standard pc-Si layers. Besides intragrain defects appearing as points (e.g. dislocation lines crossing the surface), also square shaped structures, U shaped lines and perpendicular lines are present in Figure 3. In all investigated grains where the square shaped structures, the U shaped lines and the perpendicular lines were visible after defect etching, the grains had a (001) orientation as verified by EBSD. We note that most of the grains in our pc-Si layers have a (001) orientation as a result of the AIC process. The observed structures and lines can therefore be attributed to epitaxial stacking faults along (111) planes when looking at a (001) plane [15]. From the length of the squares and the lines, we can calculate that most defects were formed in the seed layer or at the seed layer-epitaxial layer interface.

To check whether the observed intragrain defects are electrically active, we performed room-temperature EBIC measurements on our pc-Si layers after emitter diffusion. The EBIC images showed the same pattern as that found after defect etching, indicating that the crystallographic intragrain defects show a strong recombination activity [15].

Since these pc-Si layers show a large density of electrically active intra-grain defects and since V_{oc} values of these pc-Si solar cells are quasi-independent on the grain size, we believe that intra-grain defects are the major limiting factor for the electrical quality of our pc-Si layers at the moment. To decrease the number of intragrain defects, we will need to improve the AIC seed layer quality and/or optimize the epitaxial deposition process.

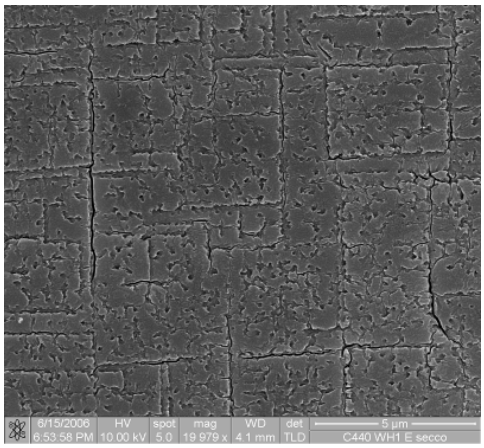

Figure 3: Top view SEM picture of a defect-etched pc-Si layer grown by thermal CVD on alumina. No grain boundaries are visible since the SEM picture was taken within one large grain.

A possible alternative to thermal CVD for the epitaxial thickening is electron beam evaporation [16, 17]. By limiting the deposition temperature to about 600°C, electron beam evaporation would allow the use of Borofloat glass as substrate. Moreover, this technique allows for high deposition rates up to 1 µm per minute and non-UHV conditions, and it is upscalable to large areas for industrial production. However, epitaxial Si deposition at temperatures as low as 600°C is very challenging.

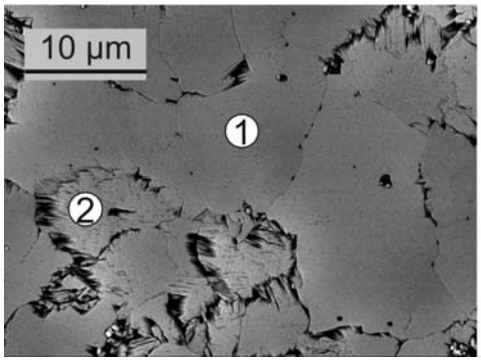

Figure 4: SEM image of a defect-etched Si film grown by electron beam epitaxy on a pc-Si seed layer at 600 °C. Grains of high (1) and low (2) quality can clearly be distinguished [18].

In order to study the influence of the underlying crystallographic orientation on the epitaxial quality, p-type silicon films (~2 µm) were grown by e-beam evaporation on monocrystalline Si wafers with (001), (101) and (111) orientations. Nearly no extended defects occurred during growth on Si(001) wafers. Epitaxial thickening of Si(101) and Si(111) wafers, however, led to many extended defects [16].

A SEM image of a defect-etched film grown at 600°C by e-beam evaporation on an AIC seed layer is shown in Fig. 4. About 60% of the grains on the sample surface exhibit a good quality epitaxial growth (1), whereas the remaining 40% shows a more defective growth (2). The good quality grains have small circular etch pits, typical for dislocations of epitaxial growth on Si(100) wafers. By EBSD measurements we could show that the good grains have a (100) orientation and that the more defective grains have other orientations [12]. These findings agree well with the EBSD measurements on ALILE seed layers (see Fig. 2 and section 3.2). The crystallographic orientation therefore has a great influence on the low-temperature epitaxy process.

As a second alternative to thermal CVD for the deposition of epitaxial absorber layers on top of AIC seed layers, we investigated layered laser crystallization [19]. After a short HF-dip, the seed layer is introduced into the evaporation chamber and heated to 500°C. A mixture of amorphous and nanocrystalline silicon is evaporated at rates up to 700 nm/min by e-beam evaporation. Doping is performed by co-evaporation of boron. After each deposition of 50 nm of silicon, the layer is irradiated by the pulse of an excimer laser (248 nm wavelength, 25 ns pulse duration, 550 mJ/cm² fluence). The laser pulse melts the newly deposited silicon and part of the crystalline layer underneath, after which the melt solidifies epitaxially starting from the crystalline layer underneath. The laser irradiation is repeated whenever 50 nm are newly deposited. The deposition is not interrupted during irradiation. In our case, a single laser spot has a dimension of 5,5x8 mm². To irradiate larger areas, the spots are scanned across the substrate. Successful epitaxial growth using LLC was recently demonstrated on AIC seed layers on Borofloat® glass.

As described elsewhere [20], epitaxial growth by LLC is independent of the orientation of the grains in the seed. This is the main advantage as compared to other low-temperature epitaxial growth methods like e-beam evaporation, since usually it is rather difficult to prepare seed layers with a perfect texture everywhere. Moreover, the defect density does not increase during the LLC thickening process. The method is rather robust, and the quality of the starting seed surface (e.g. concerning remaining oxygen atoms) is not a critical point due to the melting process.

3.4 Cell and module technology

Our best pc-Si cells so far showed an efficiency of 8.0% and are in substrate configuration with a-Si/c-Si heterojuntion emitters and interdigitated top contacts (see Fig. 5) [3]. To reach higher cell efficiencies, novel device configurations will be studied in the future, including cells in superstrate configuration with a rear junction. Simultaneously we will start the development of monolithic mini-modules.

In the near future, we will make pc-Si solar cells on glass in superstrate configuration. We will use a-Si/c-Si rear junction emitters. In order for rear junction cells to lead to good results, the diffusion length of the material needs to be several times larger than the absorber thickness. We will therefore need to enhance the diffusion length of our layers by reducing the number of intragrain defects (see section 3.3) to be able to use sufficiently thick absorber layers.

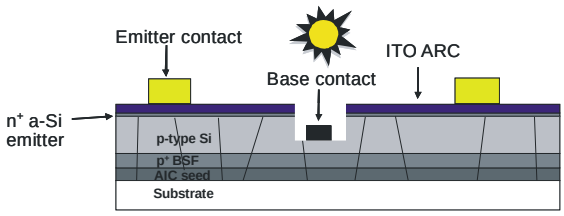

Figure 5: Schematic cross-section of pc-Si solar cells in substrate configuration.

As a first test of the feasibility of pc-Si rear junction cells based on AIC, we measured the illuminated IV parameters of an existing pc-Si cell on glass-ceramic in both substrate and superstrate configuration (see Table I). We note that the structure of this cell was optimized for the substrate configuration (see Fig. 5). The absorber layer was grown by thermal CVD and its thickness was around 2 µm. Because the as-processed devices are essentially bifacial, white paper was used as reflector in both configurations. In superstrate configuration, the current density of the cell is much lower than in substrate configuration. This is to a large extent due to the absence of an anti-reflective coating (ARC) in superstrate configuration. The difference in V_{oc} between both configurations corresponds to what is expected from the decrease in short-circuit current density [$=n \times (kT/q) \times (15.5/9.3)$]. We expect that the structure used should be able to lead to good cell results once the absorber layer thickness is optimized to the diffusion length of the material and light trapping features adapted to the superstrate configuration are applied.

Table I: The illuminated IV parameters of a pc-Si cell on a glass-ceramic, measured both in substrate and in superstrate configuration.

	J_{sc} mA/cm^2	V_{oc} mV	FF %	Eff. %
Substrate	15.5	501	67.4	5.2
Superstrate	9.3	484	68.7	3.1

We recently developed a process for pc-Si mini-modules in substrate configuration [21]. The individual cells are separated by laser grooving or alternatively by dry or wet chemical etching. The cells have an elongated shape and are connected in series by an alternating overlap of the contact fingers of one polarity with the contact fingers of opposite polarity of the next cell. To contact the base of the cells, the emitter has to be locally removed by e.g. etching. Busbars for both polarities are formed at the edges of the module. The first mini-module we made had a J_{sc} of 19 mA cm^{-2} but suffered from a shunt problem, resulting in a V_{oc} of 480 mV (120 mV /cell) and a low efficiency. The fact that the current density is the same as at cell level however shows the large potential of our mini-module process. In the near future, the reason for the shunt problem will be investigated and the module processing will be optimized to lead to much higher module efficiencies.

4 SUMMARY

We tested nanotextured Borofloat and glass-ceramic substrates and found them compatible with respectively our intermediate- and high-temperature pc-Si approaches. These glass substrates will be used in the future to obtain pc-Si solar cells in superstrate configuration.

We showed that high-quality AIC layers can be made on TCO-covered glass, which is an important result in view of obtaining cells in superstrate configuration in the intermediate-temperature route.

At present, our cell efficiency seems to be mainly limited by a high density of intragrain defects in our absorber layers. Absorber layers were grown by different epitaxial deposition methods at high- and at intermediate temperatures, and these layers were characterized by defect etching.

We measured a first cell in superstrate configuration with a V_{oc} of 484 mV. Because the structure of this cell was optimized for the substrate configuration, this result shows that rear-junction pc-Si solar cells in superstrate configuration could lead to good results. We made our first pc-Si mini-module that showed a high current density but a low efficiency due to shunting. The high current density shows that our layers are homogeneous and that good pc-Si mini-modules based on the AIC process are feasible.

5 ACKNOWLEDGEMENTS

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