DEVELOPMENT OF POLYCRYSTALLINE SILICON THIN-FILM SOLAR CELLS WITHIN THE EUROPEAN PROJECT METEOR

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ABSTRACT: The European project METEOR aims at the development of large-grained poly-Si thin-film solar cells on foreign substrates. A two step process has been used to form the poly-Si films: (1) a thin large-grained poly-Si film (seed layer) is prepared by metal-induced crystallisation (MIC) of amorphous Si and (2) this seed layer is subsequently used as a template for an epitaxial thickening process. Two different concepts have been investigated: (i) a low-temperature approach using glass substrates (T < 600 °C) and (ii) a high-temperature approach using ceramic substrates (T > 1000 °C). Using the aluminium-induced layer exchange (ALILE) process, which is based on aluminium-induced crystallisation (AIC), we have prepared p^+-type seed layers. To form also n^+-type seed layers the application of other metals has been investigated. Poly-Si thin-film solar cells have been prepared with both approaches. Using the low-temperature approach, open circuit voltages of up to 284 mV have been reached without any defect annealing or defect passivation. Using the high-temperature approach, solar cells with an efficiency of up to 5.6 % have been obtained.
Keywords: Polycrystalline, Silicon, Thin Film

1 INTRODUCTION

Thin-film solar cells on large-area foreign substrates offer a large potential for cost reduction because of (i) the reduced material consumption and (ii) the monolithic integration of the solar cells in a module. Thin crystalline silicon solar cells have the potential for very high efficiencies. This has been demonstrated by the preparation of a solar cell with an efficiency of 21.5 % on a thinned-down monocrystalline Si wafer with a thickness of 47 µm [1]. Unfortunately this is not a real Si thin-film technology but still a Si wafer technology. Therefore, a concept is required which leads to high quality Si films on foreign substrates. It is expected that such high quality Si films can be prepared using large-grained polycrystalline Si (poly-Si) with grain sizes much larger than the film thickness.

The European project METEOR ('Metal-induced Crystallisation and Epitaxial Deposition for Thin, Efficient and Low-cost Crystalline Si Solar Cells') aims at achieving this by a two step process: (1) a thin large-grained poly-Si film (seed layer) is formed by metal-induced crystallisation (MIC) of amorphous silicon (a-Si) and (2) this seed layer is subsequently used as template for an epitaxial thickening process. The corresponding schematic structure of a large-grained poly-Si thin-film solar cell on a foreign substrate is shown in Fig. 1. The p-type absorber is grown epitaxially on the p^+-type seed layer. Then a thin n^+-type emitter is formed. Finally metal contacts are deposited on both n^+-type emitter and the p-type absorber (not shown here).

Within the METEOR project two different concepts have been studied: (i) a low-temperature approach using glass substrates (T < 600 °C) and (ii) a high-temperature approach using ceramic substrates (T > 1000 °C). The low-temperature approach is characterised by a larger potential for cost reduction due to the use of inexpensive glass substrates and energy-saving process techniques while the high-temperature approach offers the faster route to efficient solar cell structures in particular due to easier epitaxial growth.

In this paper we describe the most important steps for the preparation of such large-grained poly-Si thin-film solar cells namely seed layer formation by metal-induced crystallisation and epitaxial deposition of the absorber. Finally the results of the poly-Si thin-film solar cells obtained so far are presented.

2 METAL-INDUCED CRYSTALLISATION

We have investigated the formation of large-grained poly-Si seed layers by metal-induced crystallisation of amorphous Si. Thereby we have focused mainly on the

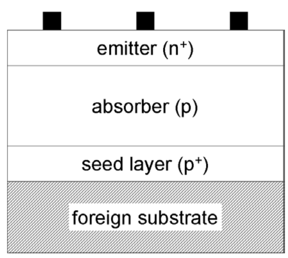

Figure 1: Schematic structure of a large-grained poly-Si thin-film solar cell on a foreign substrate. The p-type absorber is grown epitaxially on the p^+-type seed layer. On top of the p-type absorber a thin n^+-type emitter is formed.

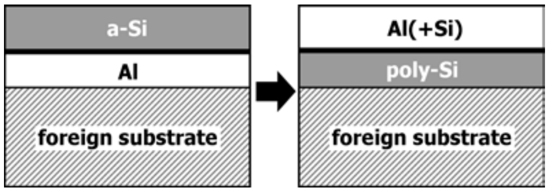

Figure 2: Schematic illustration of the ALILE process. During an annealing step the initial substrate/Al/a-Si stack is transformed into a substrate/poly-Si/Al(+Si) stack.

aluminium-induced layer exchange (ALILE) process, which is based on aluminium-induced crystallisation (AIC) [2].

The ALILE process starts with a substrate/Al/a-Si stack. Prior to the a-Si deposition the Al-coated substrate is exposed to air to form a very thin oxide layer at the Al surface. This oxide layer plays a significant role for the kinetics of the ALILE process [3]. It acts as a permeable membrane which controls the diffusion of Al and Si across the interface.

Annealing below the eutectic temperature of the Al/Si system (T_{eu} = 577 °C) leads to a transformation of the initial substrate/Al/a-Si stack into a substrate/poly-Si/Al(+Si) stack (Fig. 2). The oxide layer separates both layers throughout the process and keeps the layer thickness of the top and bottom layers constant.

The layer exchange begins with the local formation of Si nuclei within the initial Al layer. The growth of these Si nuclei is limited in vertical direction by both the substrate and the oxide layer at the initial Al/a-Si interface. However, the growth in lateral direction is not limited such that the grains grow laterally until adjacent grains coalesce and finally form a continuous poly-Si film on the foreign substrate.

The layer on top of the continuous poly-Si film contains not only Al but also ‘Si islands’ due to the fact that the initial a-Si layer is thicker than the initial Al layer which, however, is necessary to prepare continuous poly-Si films.

2.1 Low-temperature approach

For the low temperature approach the initial Al (300 nm) and a-Si (375 nm) layers were deposited by DC magnetron sputtering. Prior to the a-Si deposition the Al layer was exposed for 2h to ambient air in order to form the oxide interface layer. Annealing at 500 °C takes typically less than 2 hours. Finally, the Al(+Si) layer is completely removed by chemical mechanical polishing (CMP). The grain size is usually up to 20 µm [4].

We have investigated the surface orientation of the seed layer grains using electron back scatter diffraction (EBSD). A (100) orientation is most suitable for the subsequent epitaxial thickening at low temperatures (T < 600 °C) [5]. To characterise the seed layers a preferential (100) orientation $R_{(100)}$ is defined by the percentage of the area which is tilted by less than 20 ° with respect to the (100) orientation. In Fig. 3 $R_{(100)}$ is shown as a function of the annealing temperature T_A. It increases from about 40 % at 550 °C to about 70 % at 450 °C. A lower annealing temperature T_A thus leads to a higher preferential (100) orientation $R_{(100)}$. These observations are in agreement with the results published by Kim et al. [6]. Besides the annealing temperature other parameters such as the thickness of the membrane strongly influence the ALILE process including the preferential (100) orientation $R_{(100)}$ of the resulting seed layer. The highest values of $R_{(100)}$ observed so far amount to about 75 % [7].

2.2 High-temperature approach

For the high-temperature approach the seed layers were prepared on alumina substrates. In order to reduce the surface roughness the substrates were covered by a spin-on flowable oxide (Fox-25 from Dow Corning) prior to the seed layer formation [8]. Al and a-Si were deposited on these substrates in an electron-beam high-vacuum evaporator. In between the two depositions, the aluminium was oxidised by exposure to air for two minutes. The thickness of the Al and a-Si layers was fixed at 200 nm and 250 nm, respectively. After deposition, the samples were annealed in a tube furnace under nitrogen ambient at 500 °C for 4 hours. Finally, the top Al layer was removed by selective wet-chemical etching. The obtained seed layers had an average grain size of about 5 µm [8].

2.3 Other metals

We have searched for an equivalent to the ALILE process using other metals which may result in n^+-type seed layers. This would allow the preparation of substrate/n^+/n/p^+ solar cell structures, too. So far we did not find such an equivalent process. However, first promising results have been obtained using antimony-induced crystallisation of a-Si showing dentritic crystals with a size of up to 10 µm [9].

3 EPITAXIAL DEPOSITION

To form the absorber of the thin-film solar cell the large-grained poly-Si seed layers have been epitaxially thickened. In contrast to the seed layer formation, where the films are prepared in both approaches on different substrates but at about the same annealing temperature, the epitaxial growth of the absorber takes place in completely different temperature regimes.

3.1 Low-temperature approach

For the low-temperature approach the process steps are limited to about 600 °C because glass substrates are used. This temperature limit is very crucial to the epitaxial growth. Therefore special deposition techniques are needed which provide additional non-thermal energy

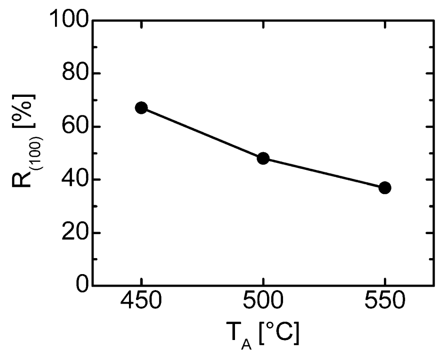

Figure 3: Preferential (100) orientation $R_{(100)}$ as a function of the annealing temperature T_A.

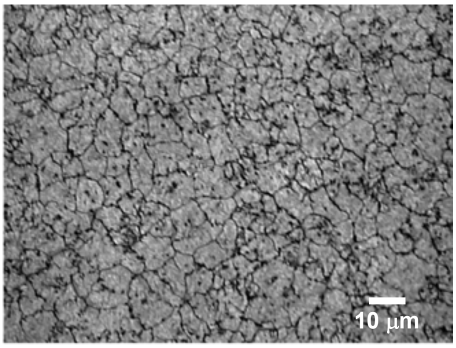

Figure 4: Optical micrograph of a typical poly-Si absorber layer after polishing and Secco etching.

to the surface of the growing film. Ion-assisted deposition techniques like electron-cyclotron resonance chemical vapour deposition (ECRCVD) have shown to be suitable to grow silicon films epitaxially at low temperatures. We have grown the p-type absorber of the solar cell by ECRCVD using silane (SiH_4) and diborane (B_2H_6). Prior to the deposition the poly-Si seed layers on glass were cleaned by a standard RCA procedure. After a final HF-dip the samples were transferred into the process chamber. During the heat-up phase the samples were held in hydrogen atmosphere. The films were grown at a substrate temperature below 600 °C with a growth rate of up to 20 nm/min.

Low-temperature epitaxy of Si in general strongly depends on the underlying crystallographic orientation. We have shown that Si films with high crystallographic quality can be grown on Si(100) wafers [5]. However, Secco defect etch experiments have clarified that the structural quality of the films has to be optimised further [7]. Substrate orientations different from (100) led to Si films with a high degree of disorder or to completely fine-crystalline growth. A detailed analysis of the influence of the grain orientation of the seed layer on the growth of the absorber is given in [10]. Due to the high preferential (100) orientation of the seed layers we have grown Si epitaxially on up to 83 % of the sample surface even at a film thickness above 1.5 μm. On the remaining area fine-crystalline Si growth has been observed.

3.2 High-temperature approach

In the high temperature approach epitaxial thickening is achieved on all crystal orientations. Absorber layers were deposited on the seed layers by thermal CVD. No attempt was made to remove the 'Si islands' from the seed layers prior to the epitaxial growth. The depositions were performed in a single-wafer epitaxial reactor (ASM Epsilon 2000) under atmospheric pressure, at a temperature of 1130 °C. The growth rate was around 1.4 μm/min.

Double layers of p^+- and p-type silicon with variable thickness ratios were made. The p^+-layer acts as additional back surface field (BSF) while the p-layer is the actual absorber layer. The total layer thickness was always between 2 and 6 μm.

The surface of the poly-Si films was too rough after epitaxial deposition for individual grains to be distinguishable. However, after mechanical polishing of the layers followed by a Secco defect etch, grain boundaries did become visible (Fig. 4). The average grain size of the poly-Si layers after epitaxial deposition was 5 μm, as determined by optical microscopy. The standard deviation was around 2.5 μm, while the largest grain size observed in these layers was about 12 μm.

4 THIN-FILM SOLAR CELLS

Poly-Si thin-film solar cell have been prepared with both low-temperature and high-temperature approach.

4.1 Low-temperature approach

In the low-temperature approach about 2 μm thick absorber layers were grown on the seed layers at 590 °C and 580 °C with boron doping of 5 ppm and 200 ppm ($[B_2H_6]/[SiH_4]$), respectively. Afterwards, an n^+-type a-Si:H emitter (about 20 nm thick) and a ZnO layer (about 80 nm thick) as transparent conductive oxide (TCO) were deposited. The area of the solar cells (about 4×4 mm^2) was defined by photolithography and wet-chemical mesa-etching. After the mesa-etching Al contacts were deposited on both the TCO and the absorber (the absorber was contacted around the mesa).

Figure 5 shows the open circuit voltages V_{oc} of both types of solar cells [7]. As-grown (state I) open circuit voltages of 61 mV and 284 mV were obtained with 5 ppm and 200ppm, respectively. So far, only the sample with a doping level of 5 ppm has received additional treatments after the absorber layer deposition. A defect annealing step (4 min at 850 °C) prior to the emitter deposition resulted in an increase of V_{oc} from 61 mV to 106 mV (state II in Fig. 5). The V_{oc} was further increased to 233 mV (state III) by an additional hydrogen passivation step (15 min at 400 °C). This shows clearly that additional treatments (defect annealing and defect passivation) are necessary to obtain reasonable open circuit voltages.

Using Ion Assisted Deposition (IAD) for the epitaxial growth Aberle et al. have reached an as-grown V_{oc} of 220 mV [11]. Thus, the as-grown V_{oc} of 284 mV is a very promising result. It is expected that additional treatments and the optimisation of the doping level will lead to a strong increase of the V_{oc}.

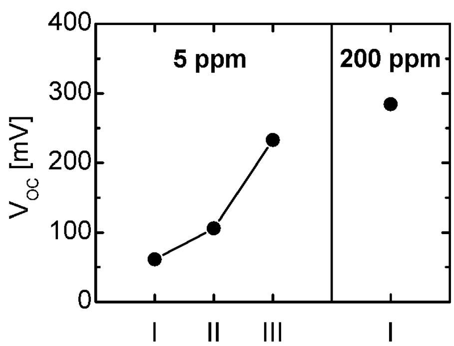

Figure 5: Open circuit voltage V_{oc} of a thin-film solar cells with different absorber doping level. The absorber layers have been grown by ECRCVD at 590 °C and 580 °C with a boron doping ($[B_2H_6]/[SiH_4]$) of 5 ppm and 200 ppm, respectively. The glass/seed layer/absorber stacks have been treated differently: state I – as grown; state II – annealed (850 °C, 4 min); state III – annealed (850 °C, 4 min) and H-passivated (400 °C, 15 min) [7].

	Jsc mA/cm^2	Voc mV	FF %	Eff. %
Best poly-Si solar cell	17.88	455	69.0	5.6

Table I: Characteristic solar cell parameters of the best poly-Si thin-film solar cell (high-temperature approach).

4.2 High-temperature approach

In the high temperature approach n^+-type emitters were formed by phosphorus diffusion from a doped pyrolithic oxide after the epitaxial deposition. Defect passivation of the layers was performed by plasma hydrogenation in a plasma enhanced CVD (PECVD) system. The details of this process are described elsewhere [12]. SiN_x layers deposited by PECVD were used as anti-reflective coating (ARC). Interdigitated metal top contacts were formed by photolithography and wet-chemical etching in combination with metal evaporation. The area of the solar cells is 1 cm^2.

The highest energy conversion efficiency achieved so far is 5.6 %. This result was obtained on a cell with an absorber doping of 3×10^{16} cm^{-3} and a thickness of 2 µm (0.5 µm BSF and 1.5 µm absorber layer). The corresponding characteristic solar cell parameters are listed in Table I. More details can be found in [13]. To our knowledge, this is the highest efficiency achieved with poly-Si thin-film solar cells on ceramic substrates where no (re)melting of Si was involved.

In general, the high-temperature absorber layers are quite homogeneous, leading to uniform cell results over large sample areas.

5 SUMMARY AND PERSPECTIVE

The present status of the European project METEOR has been presented. Large-grained poly-Si seed layers have been prepared by the ALILE process. These layers have been used as templates for epitaxial thickening at both low and high temperatures. Thin-film solar cells have been prepared for both approaches.

For the low-temperature approach an open circuit voltage of up to 284 mV has been reached without any further treatments (neither defect annealing nor defect passivation). It is expected that the application of additional treatments together with an optimisation of the boron doping level will lead to much higher open circuit voltages. Considering the early stage of the development and the big challenges due to the epitaxial growth below 600 °C the obtained V_{oc} of 284 mV is a very promising result.

In the high-temperature approach thin-film solar cells with an efficiency of up to 5.6 % have been achieved so far. Further optimisation of the seed layer quality and the cell structure should lead to much higher efficiencies.

These results show that it is possible to obtain decent efficiencies with large-grained poly-Si thin-film solar cells made by using the ALILE process. However, to be competitive to wafer-based Si solar cells, much higher efficiencies than the ones presented are needed. We strongly believe that it will be possible to obtain much better poly-Si thin-film solar cells that may ultimately lead to a cost reduction in photovoltaics.

6 ACKNOWLEDGEMENTS

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