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SILICON (REAR CONTACT) HETEROJUNCTIONS VS. DIFFUSED JUNCTIONS – CHALLENGES & BENEFITS

Delfina Muñoz

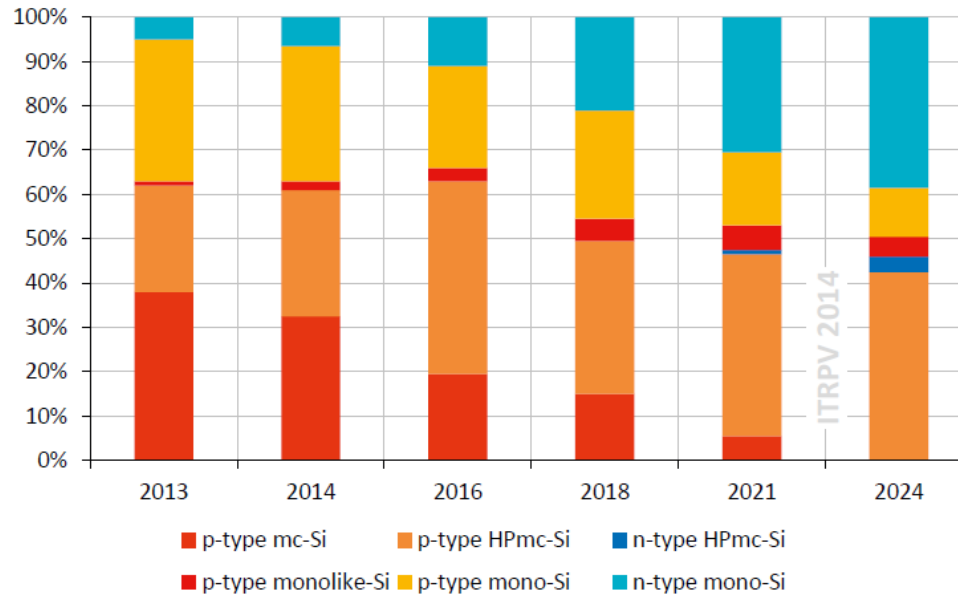


Fig. 25
Expected relative market shares for casted and mono-Si materials.

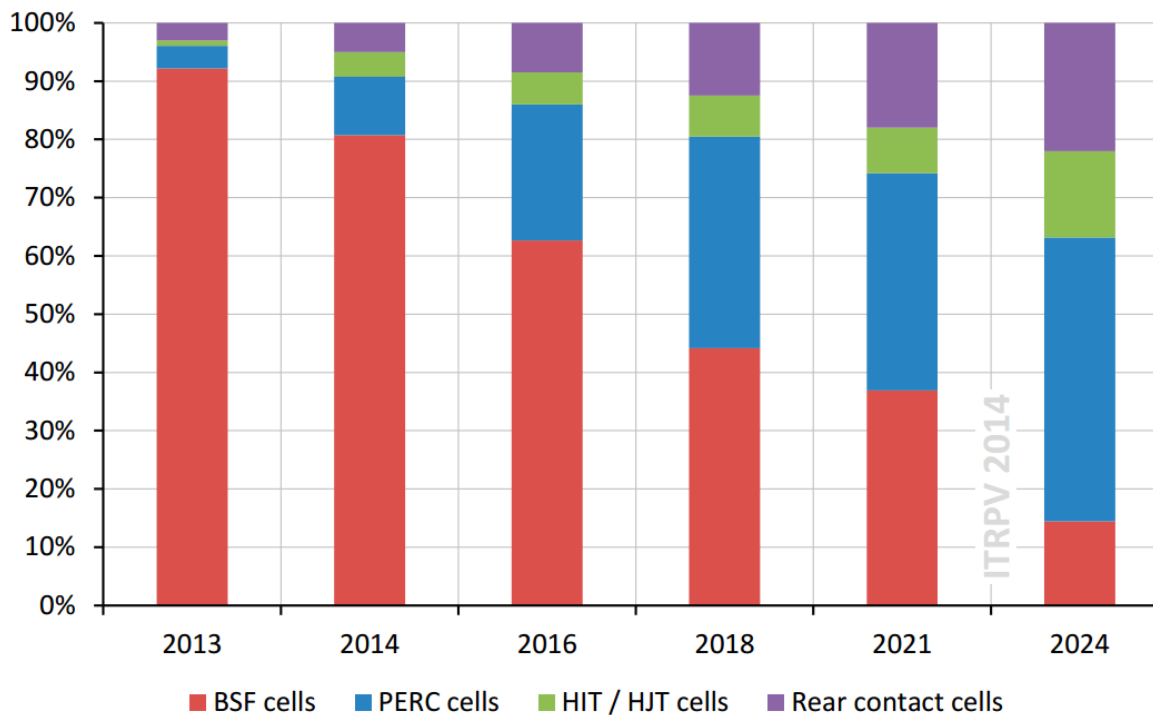
320GW on n-type!



	06/2012	12/2012	12/2013	12/2014	12/2015	12/2016	12/2017	12/2018	12/2020	12/2021	12/2023	12/2024
Cum. volume shipped (GW)	92	110	150	200	260	320	380	440	560	630	770	850



HERCULES n-type material



>100GW
In HJT technology

Nowadays
< 1GW production

> 170GW
In IBC technology

Nowadays
< 2GW production



	06/ 2012	12/ 2012	12/ 2013	12/ 2014	12/ 2015	12/ 2016	12/ 2017	12/ 2018	12/ 2020	12/ 2021	12/ 2023	12/ 2024
Cum. volume shipped (GW)	92	110	150	200	260	320	380	440	560	630	770	850



HJT in the HERCULES project



IBC in the HERCULES project

Heterojunction history vs standard solar cells

HJT vs diffused cells

Process flow: what is different?

Challenges of heterojunctions solar cells

...and diffused cells

Costs?

Towards HET-IBC: does it makes sense?

Homojunction technology

1954: Bell Labs announces the invention of the first practical silicon solar cell : 6% efficiency

D. M. Chapin, C. S. Fuller, and G. L. Pearson (May 1954). *Journal of Applied Physics* **25** (5): 676–677

1960: Hoffman Electronics : 14% efficiency

1985: University of New South Wales : 20% efficiency

2000: University of New South Wales : 25% efficiency (4cm²)

[2] M.A. Green. *Prog. Photovolt. Res. Appl.*, 17-3, 183-189 (2009)



20 years



15 years

?

Heterojunction technology

1974: Fuhs et al., first a-Si:H/c-Si heterostructures

W. Fuhs, K. Niemann and J. Stuke, *AIP Conf. Proc.* **20**, 345 (1974).

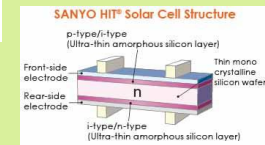
1983: Honeymoon cell a-Si:H/poly cell by Hamakawa

Y. Hamakawa, K. Fujimoto, K. Okuda, Y. Kashima, S. Nonomura and H. Okamoto, *Appl. Phys. Lett.* **43**, 644 (1983).

1984: Sanyo : 12% efficiency cell using the HJ concept

H. Matsuura, A. Matsuda, H. Okushi, T. Okuno, and K. Tanaka, *Appl. Phys. Lett.* **45**, 433 (1984).
M. Taguchi, M. Tanaka, T. Matsuyama, T. Matsuoka, S. Tsuda, S. Nakano, Y. Kishi and Y. Kuwano, *Tech. Digest 5th International Photovoltaic Science and Engineering Conference*, Kyoto, Japan, 1990, p. 689.

1990's: HIT structure by Sanyo



14.5% efficiency → Introduction of an intrinsic layer to passivate the emitter

18% efficiency and record Voc → BSF with amorphous silicon

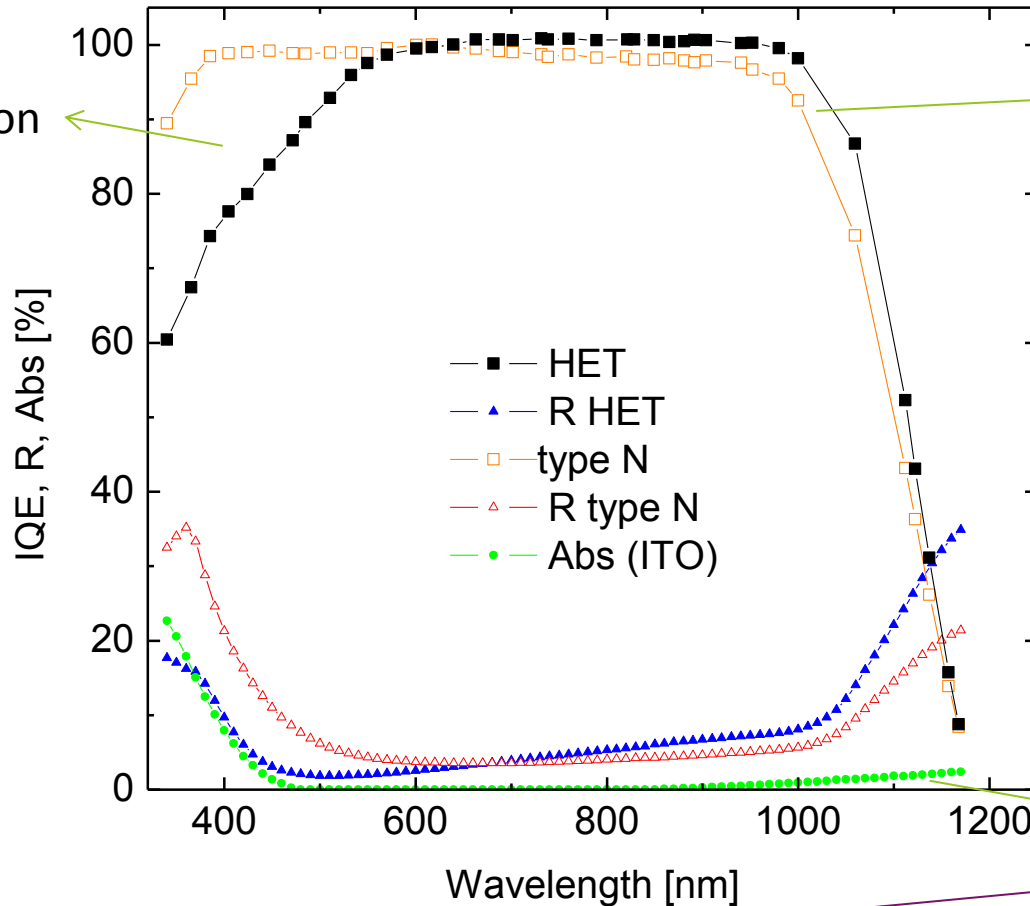
2000: 20% efficiency on large area (100cm²) by Sanyo

2014: 24.7% efficiency on large area (Sanyo)

But...

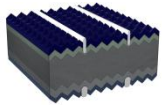
2014: Sunpower 25% IBC vs Panasonic IBC-HET 25.7%

HJT : High Voc vs difussed cells: High Jsc



optical challenge of HJT

PROCESS FLOW: what is different?



Industrial N-type PERT process (@ INES)

KOH texturing

Front Boron
diffusion

Back Phosphorous
diffusion

Thermal oxydation

Front & Back SiN

Front & Back SP

Firing

Industrial N-type HJT process (@ INES)

KOH saw dammage removal
& texturing

Cleaning & HF

Front a-Si:H layers PECVD
deposition

Back a-Si:H layers PECVD
deposition

Front & Back TCO

Front & Back SP

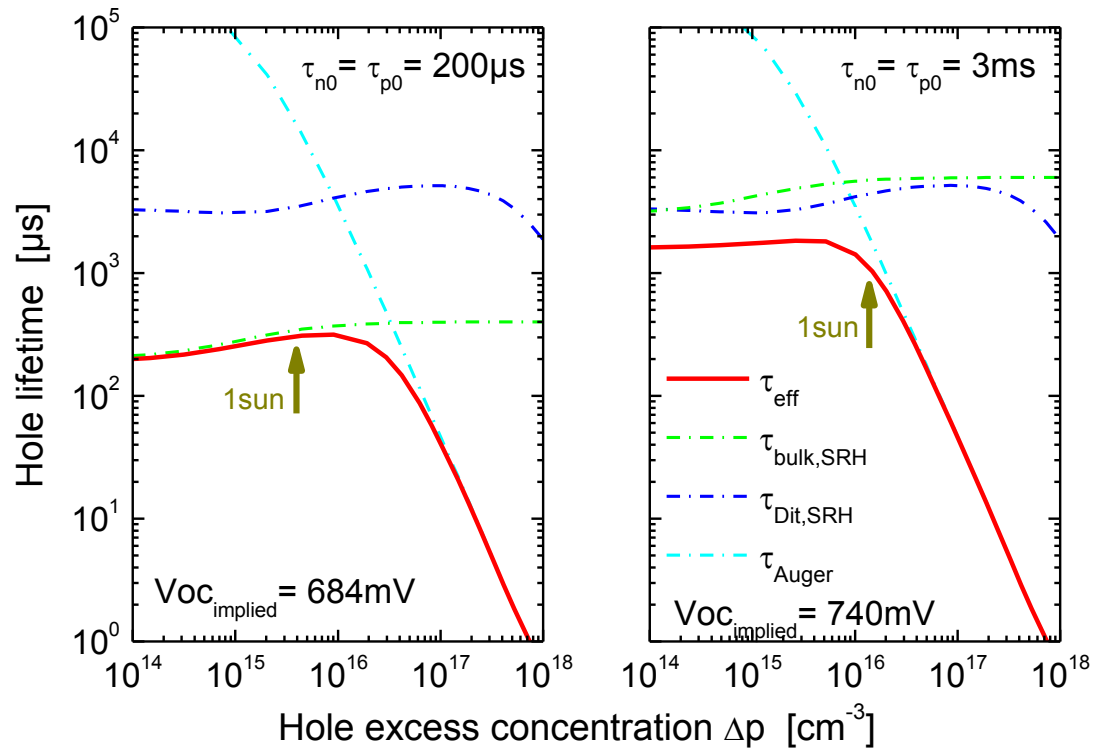
High T_p vs low T_p

→ No common steps, no common approaches,
→ limited common « know-how »



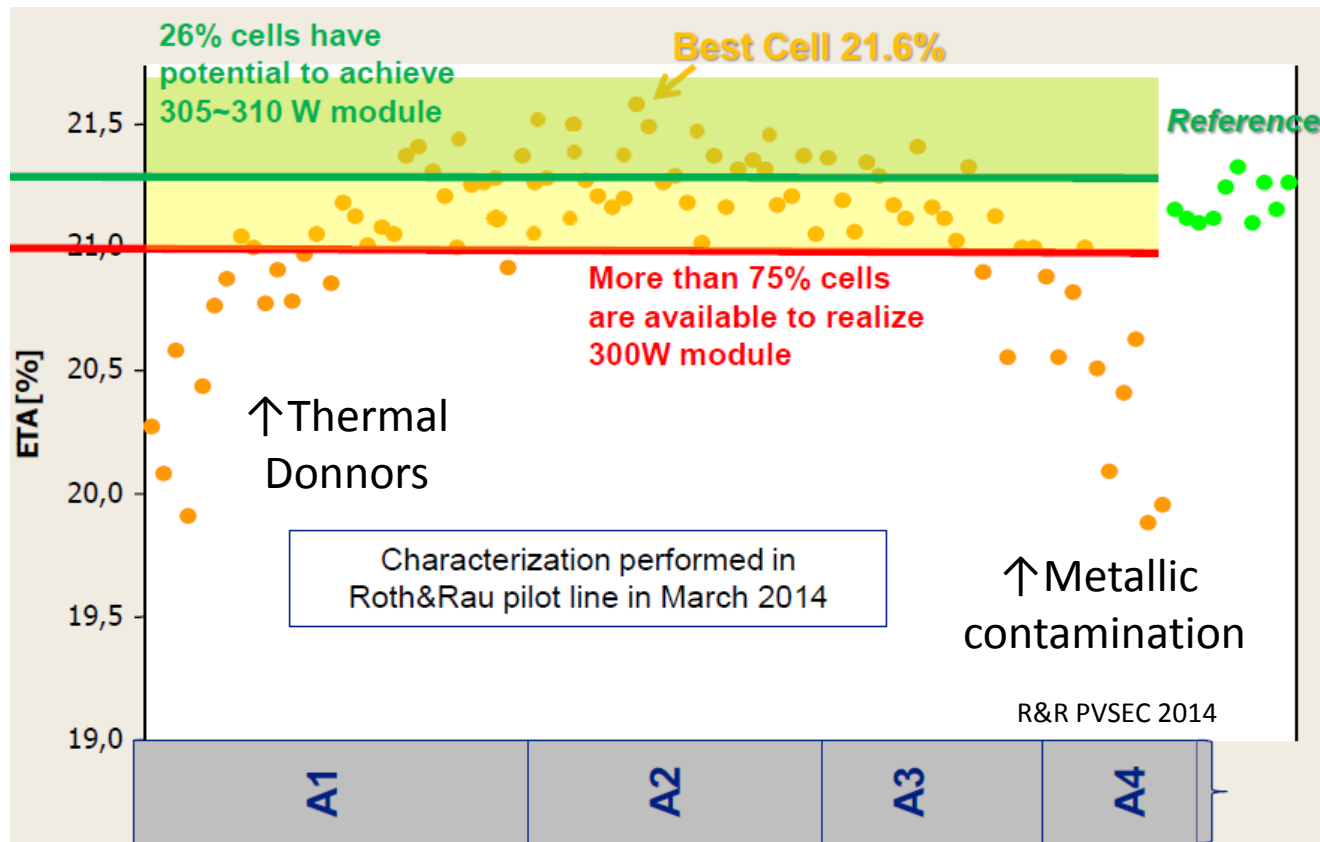
Material criticality for high Voc

Need of very high quality materials ($\tau_{\text{bulk}} > 3\text{ms}$)



Wafers cost → between 30 and 50% of cell cost for heterojunction technology when using Cz wafers

Material criticality for high Voc AND lower costs



Improve ingot use up to 100%



thermal donnors doping?

Strategy for n-type ingot doped with thermal donors

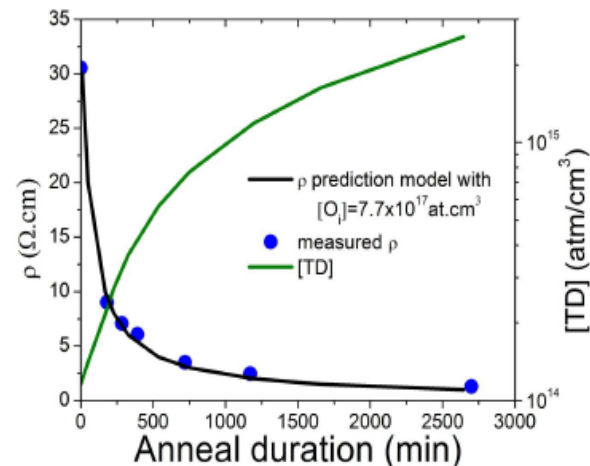
Intrinsic Cz silicon without intentional doping and high [O_i] concentration



Thermal donors activation



Resistivity control by annealing at 450°C



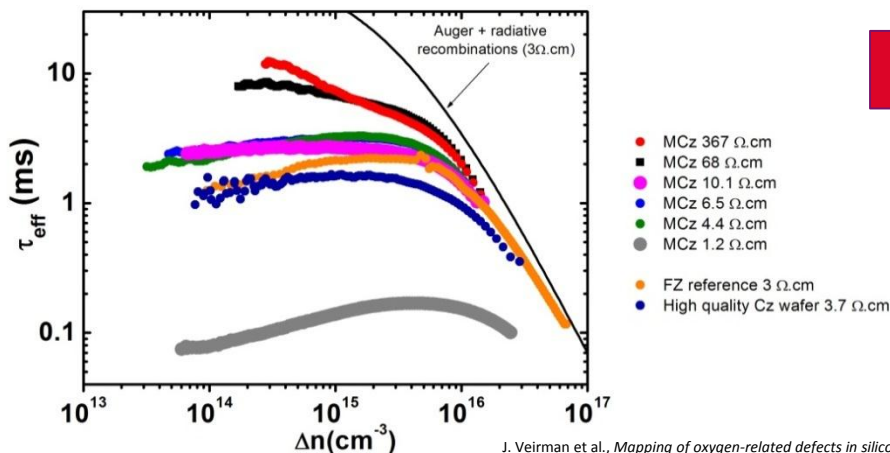
Destruction if process $T^\circ > 600^\circ\text{C}$



Compatible with HJT technology



Effective lifetime demonstrated over 3ms @ 10^{15}



J. Veirman et al., Mapping of oxygen-related defects in silicon for high efficiency solar cells : application to the prediction of LID losses, proceeding of the 28th PVSEC (2013)
 F. Jay et al., Exclusively thermal donor-doped Cz wafers for high resistivity efficiency heterojunction solar cells, Energy Procedia, 55, 533-538 (2014)
 F. Jay et al., >10ms carrier lifetimes on thermal donor-doped Cz wafers: application to heterojunction solar cells, proceeding of the 29th PVSEC(2014)

Material criticality for high Voc AND lower costs

Use of thin wafers compatible with low temperature processes (improve Voc)

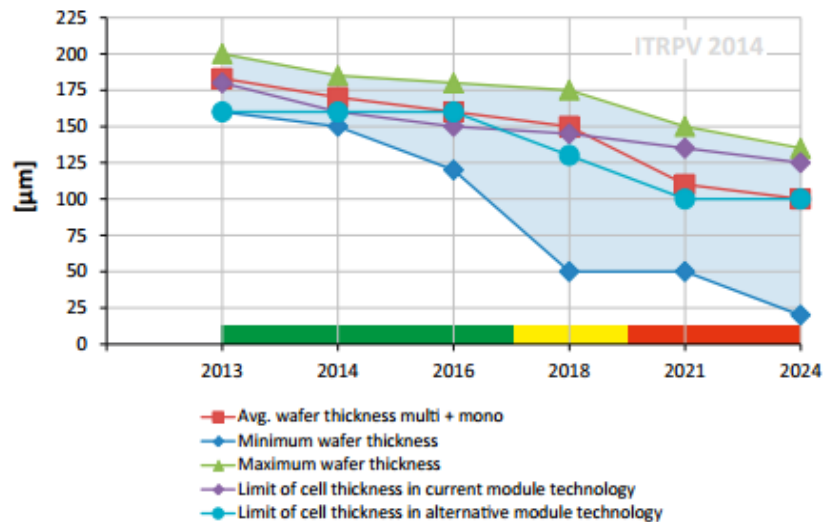


Fig. 8
 Predicted trend for minimum as-cut wafer thickness in mass production of solar cells and minimum cell thickness in module manufacturing.

→ Integration on process manufacturing

→ Absorption improvement in the IR region

Possibility of double cost reductions (€/W)

Material criticality: Silver consumption in screen-printing pastes for high efficiencies

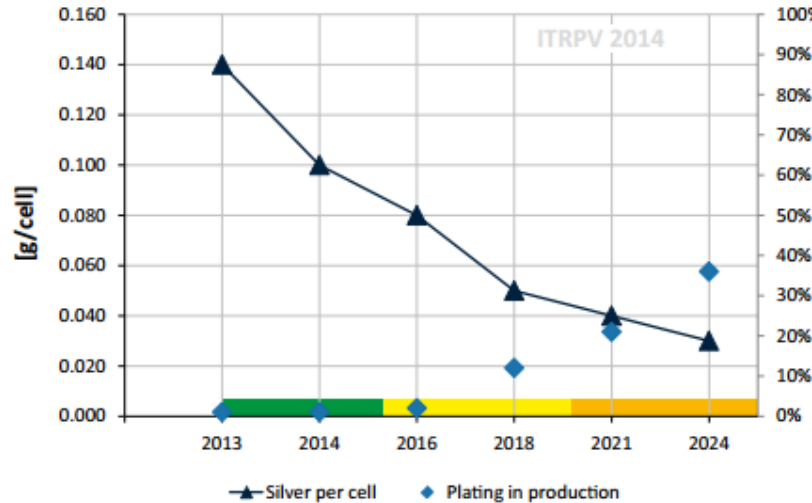


Fig. 9
Proportion of silver per cell (156x156 mm²) and the predicted share of different metallization technologies in the cell process. (Color coding refers to silver reduction).

technology		mg Ag /cell
standard HJT cells	front side	110
	bifacial	300
smart-wire HJT cells	front side	20
	bifacial	50
standard diffused cells	front side	90
	bifacial	180
smart-wire diffused cells	front side	30
	bifacial	30

Big challenge for HJT technology to reduce silver consumption in the next years to be cost competitive specially bifacial cells

- ➔ Integration of SW technology
- ➔ Patterning + Cu plating

85% Ag content in the paste
Source: INES

1. High temperature steps on material:

- Oi behavior?
- compatibility with thin wafers?
- equipment contamination?

2. How to reach high Voc?

a/ Lowly doped regions

→ Compatibility of screen-printing with low-doping profiles?

b/ recombination at metal/SC interface (J_{0met})

- Plating?
- passivated contacts?
- New generation of pastes

If high Voc: same constraints as HJT for silicon material (high lifetime > 3ms!)

3. And decrease Silver consumption, of course!

→ Less limited than HTJ

Both technologies deal with:

- Improvement on series resistance
- Improvement on pFF: edge isolation
- Production issues impacting FF (handling, wet treatments...)

&

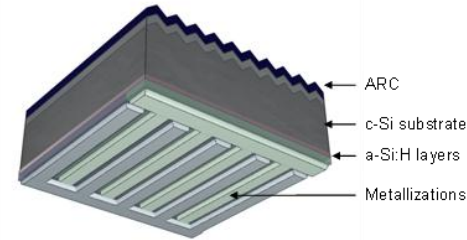
- Continuous cost reduction
- Reliability: no LID, no degradation

	Diffused cells	HJT cells
material	+ (not forget mc-Si& ML compatibility)	++
process	+	+
Metallization Ag	++	+++
Smart-wire	+	+
Cu plating	++	+
Module monofacial	PERT +	+
Module bifacial	PERC +	+

- Process HTJ cells costs are similar to n-type diffused cells except for material quality & standard BB metallization
- SW & Plating are good reduction cost vectors for HJT technology
- Bifacial module integration is a joker for both technologies

Production costs (CaPex, Opex) are driven by production capacity

World record silicon solar cells > 25% efficiency



	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)	Rdt (%)
PANASONIC (IBC HET 143 cm ²)	41,8	740	82,7	25,6
SHARP (IBC HET 4 cm ²)	41,7	736	81,9	25,1
Sunpower (IBC 121 cm ²)	41,2	730	83	25,0



23% in production

At the cell level: better short-circuit current & Voc than diffused junction
FF comparable to diffused junctions

Challenges:

- ➔ patterning of a-Si:H layers / TCO / metallization with industrial techniques
- ➔ Full wafer/large area integration
- ➔ what about costs? Will €/W & €/KWh be reasonable?
- ➔ Too many steps, big impact on costs (both CaPEX ➔ investments and OPEX ➔ wafer breakage, material)

- N-type diffused cells and heterojunctions are promising technologies but some challenges still need to be solved (the HERCULES project addresses some of them!)
- HJT vs diffused cells: No common process steps, no industrial compatibility
- HJT cells performance and cost strongly depend on material quality. TD technology can be an innovating option to assure high performances lowering costs.
- Diffused cells deals with improvements on Voc to reach higher efficiencies.
- Both technologies deal with production issues in Europe (HERCULES!)

Thanks to Yannick (n-type diffused team!)
& Pierre-Jean for their help!
Thanks to all the LHET team

Thank you for your attention!



Picture of the French National Institute for Solar Energy (INES)